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Arent Fox Kintner Plotkin & Kahn P L L C
1050 Connecticut Avenue N W Suite 600
Washington, DC 20036-5339

EXAMINER

HENN, TIMOTHY J

ART UNIT PAPER NUMBER

2612

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/654,348

Applicant(s)

SUZUKI, NOBUO

Examiner

Timothy J Henn

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-16 is/are allowed.
- 6) ☒ Claim(s) 17-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Please note that the examiner of record has changed. All future correspondence should be directed to Timothy J. Henn whose information is provided at the end of this office action.

Response to Arguments

2. Applicant's arguments with respect to claims 17-32 has been considered but are moot in view of the new ground(s) of rejection.

3. Regarding claims 33-36, the applicant argues that these claims "depend directly or indirectly from claim 17" and should be allowable for the same reasons. However, claims 33-36 are independent from claim 17. Therefore, the rejection of claims 33-36 is maintained. In the event that claim 33 is amended in a similar manner as claim 17 is currently, the examiner notes that a rejection will be made similar to the rejection of currently amended claim 17 below.

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 33-36 rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al. (US 5,306,906).

[claim 33]

Referring to claim 33, Aoki discloses a method of driving the solid-state image pickup device in figures 1A and 5 comprising a semiconductor substrate 101; a large number of photoelectric converters 3 arranged on one surface of said semiconductor substrate 101 in a plurality of columns and a plurality of rows, each of said columns and said rows including a plurality of photoelectric converters 3, said photoelectric converters 3 in odd ones of said columns being shifted about one half of a pitch P, in a direction of said column relative to said photoelectric converters 3 in even ones of said columns, said photoelectric converters 3 in odd ones of said rows being shifted about one half of a pitch P2 in a direction of said row relative to said photoelectric converters in even ones of said rows, each said photoelectric converter column including said photoelectric converters 3 of only said odd rows or said even rows; a vertical charge transfer channel provided for each said photoelectric converter column on the surface of said semiconductor substrate 101, each said channel being adjacent to an associated photoelectric converter column, each said channel including a plurality of sections of different directions lying in a line, said channel generally extending, while meandering in a zigzag shape, in column direction; a plurality of transfer electrodes 1 and 2 disposed on the surface of said semiconductor substrate 101 to intersect in plan view said charge transfer channels, each said transfer electrode 1 and 2 including a plurality of transfer path forming regions which are equal in number to said charge transfer channels, each said transfer path forming region covering one of said sections of said charge transfer channels, said transfer path forming region and said section disposed there under forming one charge transfer stage 2 and 12; each said transfer electrode generally

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extending in row direction, while two adjacent ones of said transfer electrodes sandwiching one of said photoelectric converter rows there between and determining one photoelectric converter region for every second one of said photoelectric converter columns by meeting each other and parting from each other to enclose in plan view every one of said photoelectric converters in said odd or even row; and a readout gate region disposed 112 contiguous to each said photoelectric converter and to an associated one of said charge transfer channels, said readout gate regions being equal to each other in relative positional relationship with said associated photoelectric converter 3, each said readout gate region associating to one of said photoelectric converter rows being covered in plan view with mutually different ones of said transfer path forming regions 12(6) of said one transfer electrode 1 and 2 associating to said photoelectric converter row, comprising the steps of: reading out, in one vertical blanking period, signal charge stored in each said photoelectric converter of at least part of said photoelectric converter rows, via said associated readout gate region 112 contiguous to said photoelectric converter 3, to said associated charge transfer channel contiguous to said associated readout gate region; and converting, from the vertical blanking period to a next vertical blanking period subsequent thereto, each said signal charge read out to said charge transfer channel into an image signal and outputting the image signal.

[claim 34]

Referring to claim 34, Aoki discloses a solid-state image pickup device driving method, wherein said charge transfer channels and said transfer electrodes configure at least two charge transfer stages 11 and 12 for each said photoelectric converter.

[claim 35]

Referring to claim 35, Aoki discloses a solid-state image pickup device driving method, wherein said transfer electrodes include a plurality of first transfer electrodes 1 and a plurality of second transfer electrodes 2, said first and second transfer electrodes 1 and 2 being alternately provided on the surface of said semiconductor substrate to intersect in plan view said charge transfer channels, each said first and second transfer electrode 1 and 2 including a plurality of transfer path forming regions which are equal in number to said charge transfer channels, each said transfer path forming region 2 and 12 covering one of said sections of said charge transfer channels, said transfer path forming region and said section disposed there under forming one charge transfer stage; each said first and second transfer electrode 1 and 2 generally extending in row direction, while one of said first transfer electrodes 1 and one of said second transfer electrodes 2 adjacent to said one first transfer electrode sandwiching one of said photoelectric converter rows there between and determining one photoelectric converter region for every second one of said photoelectric converter columns by meeting each other and parting from each other to enclose in plan view every one of said photoelectric converters in said odd or even row.

[claim 36]

Referring to claim 36, Aoki discloses a solid-state image pickup device driving method, wherein each said readout gate region 112 contiguous to odd one of said charge transfer channels 12 is contiguous to said section covered with said transfer path forming region of said first transfer electrode, and each said readout gate region 112 contiguous to even one of said charge transfer channels is contiguous to said section covered with said transfer path forming region of another one of said first transfer electrodes 1.

6. Claims 37 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (JP 10-136391).

[claim 37]

Regarding claim 37, Yamada discloses a solid-state image pickup device comprising: a semiconductor substrate (Figure 8); a multiplicity of photodiodes formed in the substrate (Figure 8, Items 31a - 35c) and configured in row and column matrix shape including a first tetragonal row and column matrix (Figure 8, Items 31a - 33d), and a second row and column matrix disposed at interstitial positions of the first tetragonal matrix (Figure 8, Items 34a - 35c); a plurality of charge transfer channels formed in the semiconductor substrate, disposed adjacent to the columns of the row and column matrix, extending in the column direction as a whole and locally meandering around the photodiodes (Figure 8, Items 36a - 37c); a multiplicity of readout gate regions formed in said semiconductor substrate, each readout gate region disposed between an associated one of the photodiodes and an associated one of the charge

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transfer channels so that a positional relationship between each readout gate region and the associated photodiode and the associated vertical transfer channel is the same for all readout gate regions (Figure 8, arrows; Paragraphs 0016-0017; The examiner notes that in order for the photodiodes to readout charge to the vertical transfer channels, a readout gate region must inherently be disposed in the area of the arrows of each photodiode in Figure 8); and a plurality of transfer electrodes disposed above the semiconductor substrate along the row direction in such a manner that two transfer electrodes extend on both sides of each row of the photodiodes, crossing the charge transfer channels, and constituting two transfer stages for each charge transfer channel (Figure 8, Items 39a - 42b; The examiner notes that the presence of a transfer electrode above the vertical transfer channel inherently defines a transfer stage in the vertical transfer channel, and that two adjacent electrodes (e.g. Figure 8, Items 39b and 40b) would inherently form two transfer stages in the charge transfer channels as claimed); wherein each readout gate region is adjacent to one transfer stage of the associated charge transfer channel (Figure 8, arrows).

[claim 40]

Regarding claim 40, Yamada discloses the use of four pulses in the form of first, second, third and fourth clocks which are applied to the transfer electrodes 39a - 42b (Paragraph 0019). The examiner notes that pulse supply terminals must inherently be included for the transfer pulses to be applied to the transfer electrodes.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 17-30 and 37-39 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 5,306,906) in view of Yamada (JP 10-136391 A).

[claim 17]

Referring to claim 17, Aoki discloses a solid-state image pickup device in figures 1A and 5, comprising; a semiconductor substrate 101; a large number of photoelectric converters 3 arranged on one surface of said semiconductor substrate 101 in a plurality of columns and a plurality of rows, each of said columns and said rows including a plurality of photoelectric converters 3, said photoelectric converters in odd ones of said columns being shifted about one half of a pitch P, in a direction of said column relative to said photoelectric converters in even ones of said columns, said photoelectric converters 3 in odd ones of said rows being shifted about one half of a pitch P2 in a direction of said row relative to said photoelectric converters 3 in even ones of said rows, each said photoelectric converter column including said photoelectric converters 3 of only said odd rows or said even rows; a vertical charge transfer channel provided for each said photoelectric converter column on the surface of said semiconductor substrate 101, each said channel being adjacent to an associated photoelectric converter column, each said channel including a plurality of sections of different directions lying in a line, said channel generally extending, while meandering in a zigzag shape, in column direction; a plurality of transfer electrodes 1 and 2 disposed on the

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surface of said semiconductor substrate 101 to intersect in plan view said charge transfer channels, each said transfer electrode 1 and 2 including a plurality of transfer path forming regions which are equal in number to said charge transfer channels, each said transfer path forming region covering one of said sections of said charge transfer channels, said transfer path forming region 12(6) and said section disposed there under forming one charge transfer stage; each said transfer electrode generally extending in row direction, while two adjacent ones of said transfer electrodes 1 and 2 sandwiching one of said photoelectric converter rows there between and determining one photoelectric converter region for every second one of said photoelectric converter columns by meeting each other and parting from each other to enclose in plan view every one of said photoelectric converters in said odd or even row; and a plurality of readout gate regions 112 wherein each readout gate region is disposed contiguous to an associated one of said photoelectric converters 3 in figure 5 and to an associated one of said charge transfer channels, each said readout gate region 112 associating to one of said photoelectric converter rows being covered in plan view with mutually different ones of said transfer path forming regions 12(6) of said one transfer electrode associating to said photoelectric converter row. However Aoki does not disclose readout gate regions wherein each one of said readout gate regions is equal to each other in relative positional relationship with said associated photoelectric converter.

Yamada teaches associating a readout region for each photoelectric converter in the same relative positional relationship as all of the other readout regions and photoelectric converters so that even if a positional displacement occurs, the distance

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from each photo sensor to the column direction charge transfer devices changes by the same amount for all photo sensors because all signal charges are read only in a single direction (Paragraphs 0016-0017). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to align all photoelectric converters and readout regions in the same relative positional relationship so that high precision alignment is not required during the manufacture of the solid-state image pickup device.

[claim 18]

Referring to claim 18, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein said charge transfer channels and said transfer electrodes 1 and 2 configure at least two charge transfer stages 5 for each said photoelectric converter.

[claim 19]

Referring to claim 19, Aoki in view of Yamada discloses A solid-state image pickup device shown in figures 1A and 5, wherein said transfer electrodes 1 and 2 include a plurality of first transfer electrodes 1 and a plurality of second transfer electrodes 2, said first and second transfer electrodes 1 and 2 being alternately provided on the surface of said semiconductor substrate 101 to intersect in plan view said charge transfer channels, each said first and second transfer electrode 1 and 2 including a plurality of transfer path forming regions 12 and 22 which are equal in number to said charge transfer channels, each said transfer path forming region 12 and 22 covering one of said sections of said charge transfer channels, said transfer path

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forming region 12 and 22 and said section disposed there under forming one charge transfer stage 5; each said first and second transfer electrode 1 and 2 generally extending in row direction, while one of said first transfer electrodes and one of said second transfer electrodes adjacent to said one first transfer electrode sandwiching one of said photoelectric converter rows there between and determining one photoelectric converter region for every second one of said photoelectric converter columns by meeting each other and parting from each other to enclose in plan view every one of said photoelectric converters in said odd or even row.

[claim 20]

Referring to claim 20, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein: each said readout gate region 112 6 contiguous to an odd one of said charge transfer channels is contiguous to said section covered with said transfer path forming region of said first transfer electrode 1, and each said readout gate region 112 6 contiguous to even one of said charge transfer channels is contiguous to said section covered with said transfer path forming region of another one of said transfer electrodes.

[claim 21]

Referring to claim 21, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, further including a plurality of readout gate electrode regions 12(6), said readout gate electrode region 12(6) being disposed on each said readout gate region 112 and covering said readout gate region 112 in plan view, wherein each said readout gate electrode region 12(6) is a part of said transfer

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path forming region covering in plan view one of said section of said charge transfer channel contiguous to said readout gate region associating to said readout gate electrode region.

[claim 22]

Referring to claim 22, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein said photoelectric converters are substantially equal to each other in contour, size, and direction in plan view.

[claim 23]

Referring to claim 23, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein each said photoelectric converter region determined by said two adjacent transfer electrodes sandwiching said one photoelectric converter column there between has a contour of substantially a hexagon in plan view.

[claim 24]

Referring to claim 24, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, further including a light shielding film 111 having an opening provided for each said photoelectric converter 3, each said opening being disposed over the associated photoelectric converter 3.

[claim 25]

Referring to claim 25, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein said openings are substantially equal to each other in contour, size, and direction in plan view.

[claim 26]

Referring to claim 26, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, wherein each said opening has a contour equal to a hexagon in plan view.

[claim 27]

Referring to claim 27, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, further including a microlens provided for each said opening, each said microlens 108 in figures 6A and 6B being disposed over the associated opening and covering the opening in plan view.

[claim 28]

Referring to claim 28, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, but does not further include a color filter provided for each region between said opening and said microlens shown in figures 6A and 6B associating to the opening, said color filter covering the associated opening in plan view. However, Official Notice is taken that providing a color filter for each pixel sensor is well known. Therefore it would have been obvious to provide a color filter at each opening for each pixel sensor so as to capture images in color instead of only monochrome.

[claim 29]

Referring to claim 29, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, further including a driver circuit (not shown) for applying filed shift pulses respectively to said transfer electrodes 1 and 2 of which said

transfer path forming regions cover said readout gate regions in plan view (Col. 5, Lines 26 – 44).

[claim 30]

Referring to claim 30, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5, further including a driver circuit (not shown) for applying filed shift pulses respectively to said first and second transfer electrodes 1 and 2 (Col. 5, Lines 26 – 44).

[claim 37]

Regarding claim 37, Aoki discloses a solid-state image pickup device comprising: a semiconductor substrate (Figure 5, Item 101); a multiplicity of photodiodes formed in the substrate (Figure 1A, Items 3) and configured in row and column matrix shape including a first tetragonal row and column matrix, and a second row and column matrix disposed at interstitial positions of the first tetragonal matrix (Figure 1A); a plurality of charge transfer channels formed in the semiconductor substrate, disposed adjacent to the columns of the row and column matrix, extending in the column direction as a whole and locally meandering around the photodiodes (Figure 1A, Items 5); a multiplicity of readout gate regions formed in said semiconductor substrate, each readout gate region disposed between an associated one of the photodiodes and an associated one of the charge transfer channels (Figure 1A, Items 6; Figure 5, Item 112); and a plurality of transfer electrodes disposed above the semiconductor substrate along the row direction in such a manner that two transfer electrodes extend on both sides of each row of the photodiodes, crossing the charge transfer channels, and constituting two transfer stages

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for each charge transfer channel (Figure 1A, Items 11, 12, 21 and 22; Figure 5, Item 12(6)) would inherently form two transfer stages in the charge transfer channels as claimed); wherein each readout gate region is adjacent to one transfer stage of the associated charge transfer channel (Figure 1A, Items 6; Figure 5, Item 112). However, Aoki does not disclose positioning the readout gate regions of the photodiodes such that a positional relationship between each readout gate region and the associated photodiode and the associated vertical transfer channel is the same for all readout gate regions.

Yamada teaches associating a readout region for each photodiode in the same relative positional relationship as all of the other readout regions and photoelectric converters so that even if a positional displacement occurs, the distance from each photo sensor to the column direction charge transfer devices changes by the same amount for all photo sensors because all signal charges are read only in a single direction (Paragraphs 0016-0017). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to align all photodiodes and readout regions in the same relative positional relationship so that high precision alignment is not required during the manufacture of the solid-state image pickup device.

[claim 38]

Regarding claim 38, the transfer electrodes of Aoki in view of Yamada would constitute one transfer stage for each charge transfer channel, and continuously covers the readout gate region for every two transfer channels (Figure 1A; Figure 5, Items 112 and 12(6)); The examiner notes that if the readout gate regions were aligned as taught

by Yamada in Figure 1A, they would be covered by a transfer electrode as claimed).

[claim 39]

Regarding claim 40, the transfer channels of Aoki have a constant width (Figure 1A, Items 5).

9. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 5,306,906) in view of Yamada (JP 10-136391 A) as applied to claim 17 above, and in further view of Sekine (US 4,602,289).

[claim 31]

Referring to claim 31, Aoki in view of Yamada discloses a solid-state image pickup device shown in figures 1A and 5 but does not specifically show the output means of the sensor. However, Sekine discloses an image sensor in figure 1 further including an output transfer path 30 being composed of a CCD of two-phase driving type with two-layer electrode structure, said output transfer path 30 receives, via said charge transfer channels, signal charge stored in each said photoelectric converter through photoelectric conversion conducted by said each photoelectric converter and transfers said signal charge in a predetermined direction.

Therefore it would have been obvious to provide the output transfer path of Sekine with the image sensor of Aoki in view of Yamada so that charges can be output from the image sensor to form an electronic image.

[claim 32]

Referring to claim 32, Sekine discloses a solid-state image pickup device shown in figure 1 further including an adjusting section 260, said adjusting section 260

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including an adjusting charge transfer channel for each said charge transfer channel connected to one end thereof, said adjusting charge transfer channels changing, before said signal charge is transferred to said output transfer path 30, the transfer direction of said signal charge and adjusting mutual pitch in said photoelectric converter row direction to a constant value.

10. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (JP 10-136391 A) in view of Sakota et al. (US 5,376,967).

[claim 41]

Regarding claim 41, Yamada teaches the use of four-phase driving methods as is well known in the art, but does not disclose the specifics.

Sakota teaches a four-phase driving method in which a drive circuit supplies signals to transfer electrodes in which at least two readout pulse signals to at least two of the four pulse supply terminals are simultaneously driven activating at least two adjacent transfer electrodes (Figures 2 and 3A). The driving method of Sakota allows dark currents to be suppressed (c. 4, ll. 38-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the driving method of Sakota in order to suppress the occurrence of dark currents.

Allowable Subject Matter

11. Claims 1 – 16 are allowed.

[claims 1-16]

The following is a statement of reasons for the indication of allowable subject matter:

Referring to claims 1 and 14, the prior art fails to teach or suggest each charge transfer channel having a first width at the location where the channel is contiguous to the readout gate region and a second width at a location where the channel is separated from the readout gate where the first width is less than the second width.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is an English language equivalent to the cited Japanese Yamada reference:

i. Yamada US 6,236,434

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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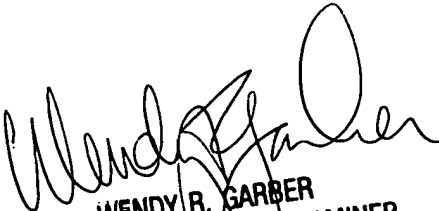
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Henn whose telephone number is (703) 305-8327 or (571) 272-7310 after 28 February 2005. The examiner can normally be reached on M-F 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJH
1/25/2005


WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600